MOSFET Silicon N-Channel MOS

1. Applications

Soft Switching Boost PFC switch, Half bridge or Asymmetric half bridge or Series resonance half bridge and
full bridge topologies.
phase-shift-bridge(ZVS),LLC Application-Server Power,
Telecom Power, EV Charging, Solar inverter.

2. Features

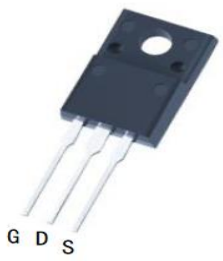
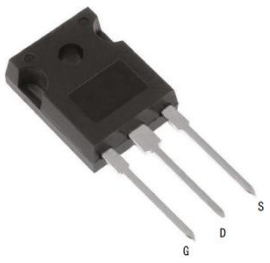
Low drain-source on-resistance: RDS(ON) = 0.080Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 3 to 5V

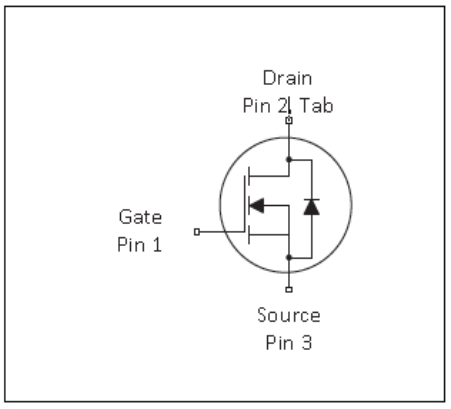
Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	90	mΩ
$Q_{g,typ}$	65.32	nC
$I_{D,pulse}$	141	A
Body diode dv/dt	50	V/ns

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASA60R090EFDA	TO220F	ASA60R090EFDA
ASW60R090EFDA	TO247-3L	ASW60R090EFDA

TO220F	TO247-3L
	



1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D		-	47	A	T_C=25°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	141	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	885	mJ	Tc=25°C, V_{DD}=50V, L=10mH, RG=25Ω
MOSFET dv/dt ruggedness	dv/dt	-	-	59	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	191	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Soldering Temperature Distance of 1.6mm from case for 10s	T_L			260	°C	
Reverse diode dv/dt[3)]	dv/dt	-	-	50	V/ns	V_{DS}=0...400V, I_{SD}<=48A, T_j=25°C see table 8

[1)] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2)] Pulse width t_p limited by $T_{j,max}$
[3)] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics (TO220F)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.65	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	device on PCB, minimal footprint

Thermal characteristics (TO247)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.65	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	605	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{(GS)th}$	3		5	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	5	uA	V_{DS}=600V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.080	0.090	Ω	V_{GS}=10V, I_D=20A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	0.9	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3291	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Output capacitance	C_{oss}	-	298.1	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Reverse transfer capacitance	C_{rss}	-	10.7	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Turn-on delay time	$t_{d(on)}$	-	12.1	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=25.8A R_G=1.7Ω;see table 9
Rise time	t_r	-	4.4	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=25.8A R_G=1.7Ω;see table 9
Turn-off delay time	$t_{d(off)}$	-	39.1	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=25.8A R_G=1.7Ω;see table 9
Fall time	t_f	-	4.3	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=25.8A R_G=1.7Ω;see table 9

Table 6 Gate charge characteristics

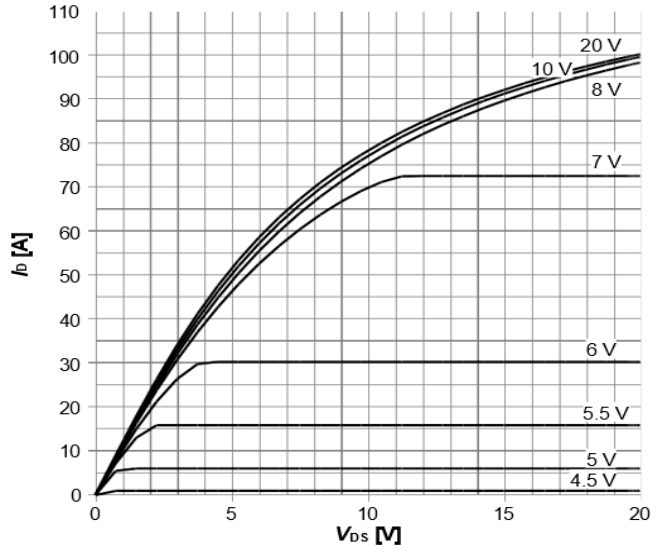
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	18.16	-	nC	V_{DD}=400V, I_D=25.8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	22.93	-	nC	V_{DD}=400V, I_D=25.8A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	65.32	-	nC	V_{DD}=400V, I_D=25.8A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.98	-	V	V_{DD}=400V, I_D=25.8A, V_{GS}=0 to 10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.66	-	V	V_{GS}=0V, I_F=1A, T_j=25°C
Reverse recovery time	t_{rr}	-	147.8	-	ns	Vr=400v,IF=9.6A,di/dt=100A/us see table 8
Reverse recovery charge	Q_{rr}	-	0.96	-	uC	Vr=400v,IF=9.6A,di/dt=100A/us see table 8
Peak reverse recovery current	I_{rrm}	-	12.27	-	A	Vr=400v,IF=9.6A,di/dt=100A/us see table 8

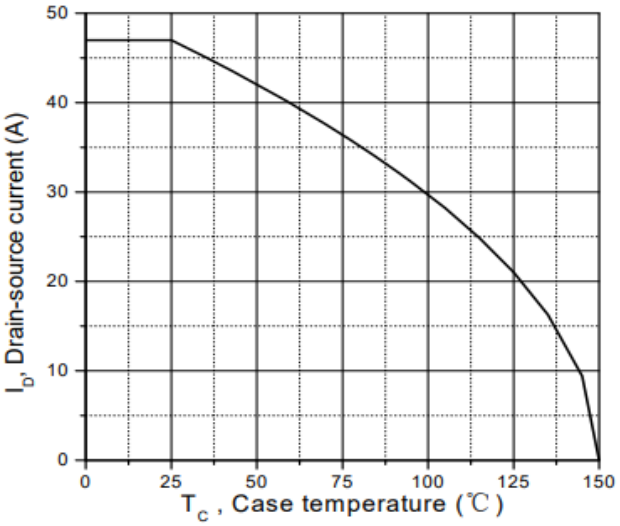
4 Electrical characteristics diagram

Diagram 1: Typ. Output characteristics



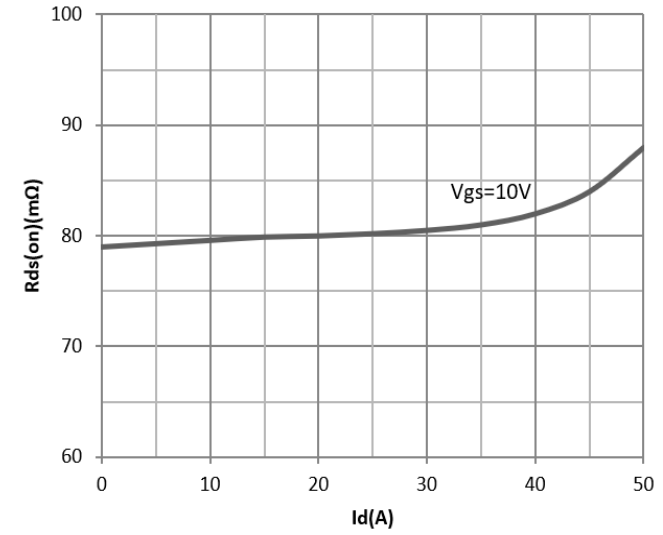
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}

Diagram 2: Typ. Drain Current De-rating



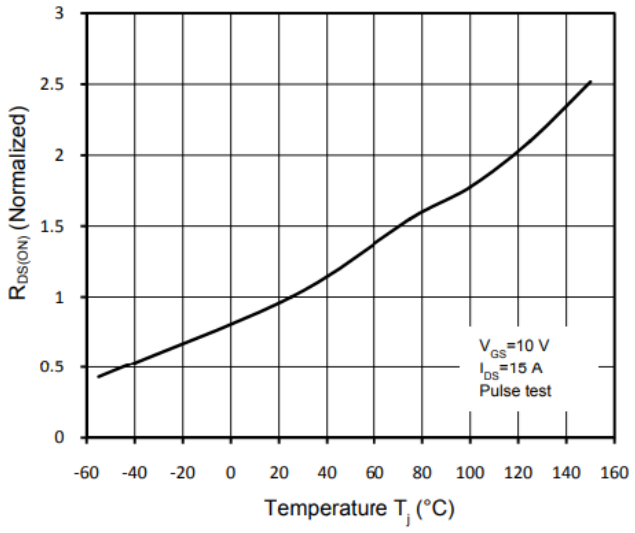
Id=f(T_C);

Diagram 3: Typ. Rdson vs. Drain Current



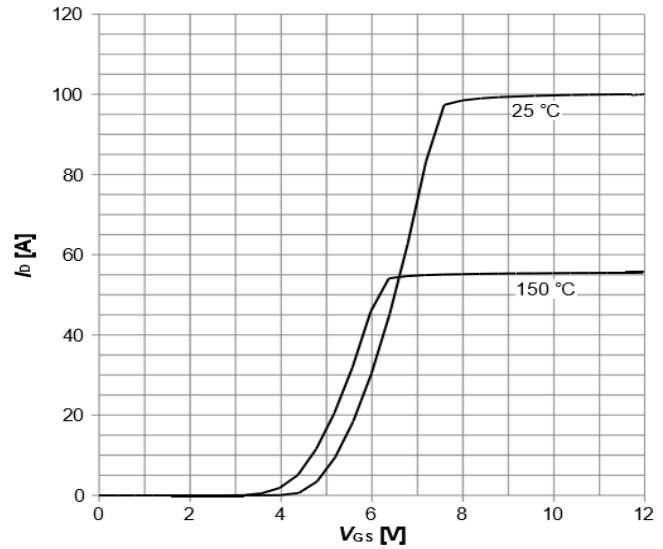
$R_{ds(on)}$=f(*Id*);Vgs=10V

Diagram 4: Typ. Rdson – Junction Temperature



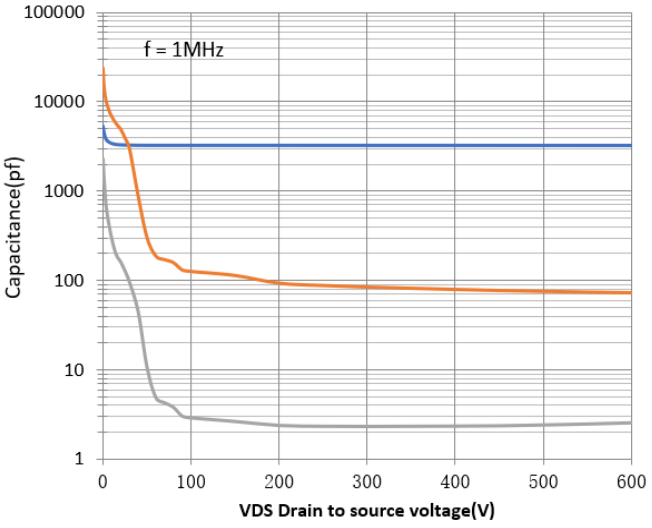
$R_{ds(on)}$=f(T_j);Vgs=10V/I_D=15A

Diagram 5: Typ. transfer characteristics



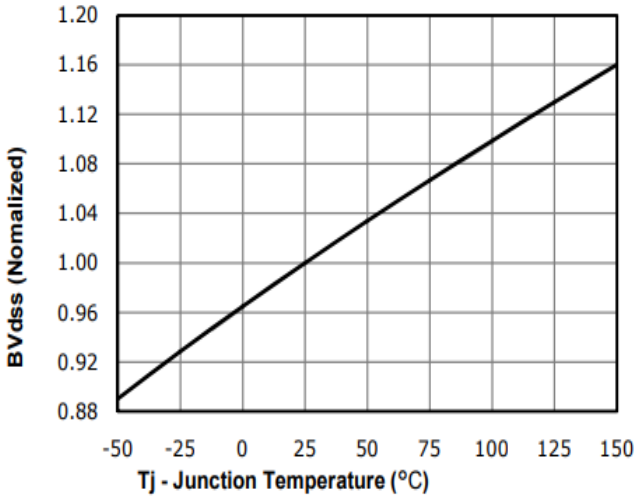
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 6: Typ. Capacitance vs. Vds



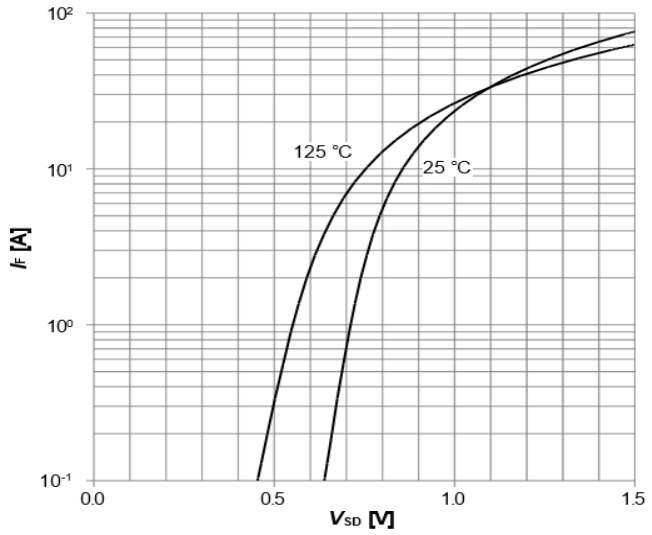
C=f(V_{DS});V_{GS}=0V; f=1MHz

Diagram 7: Typ. BVDSS voltage vs. Temperature



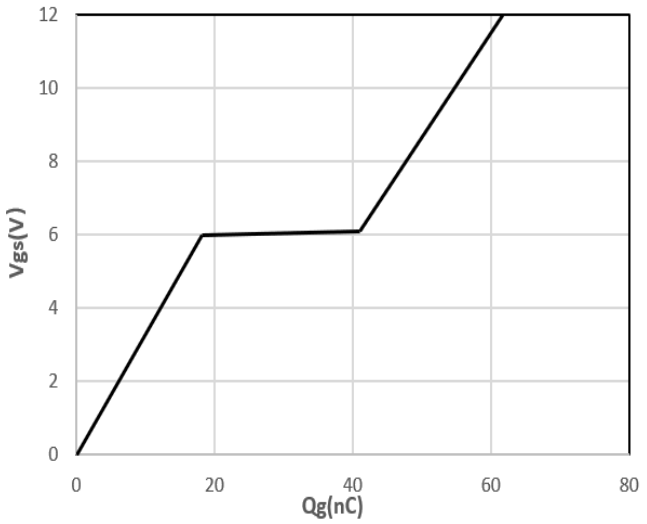
V_{GS}=f(Tj);I_D=250uA

Diagram 8: Typ. Source-Drain Diode Forward



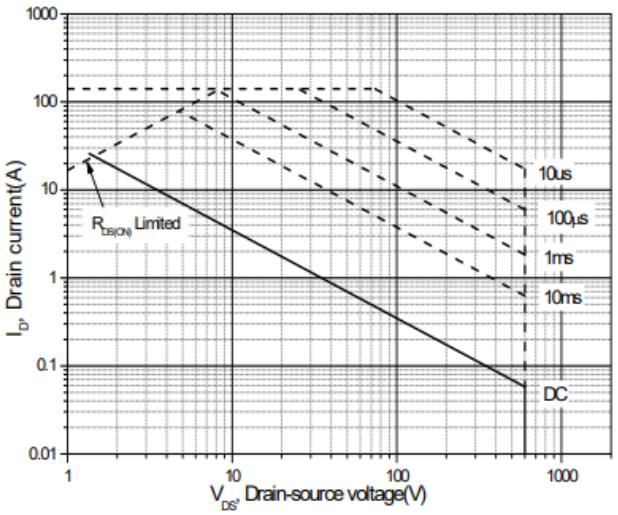
I_{SD}=f(V_{DS}); T_C=25 °C;

Diagram 9: Typ. Gate charge



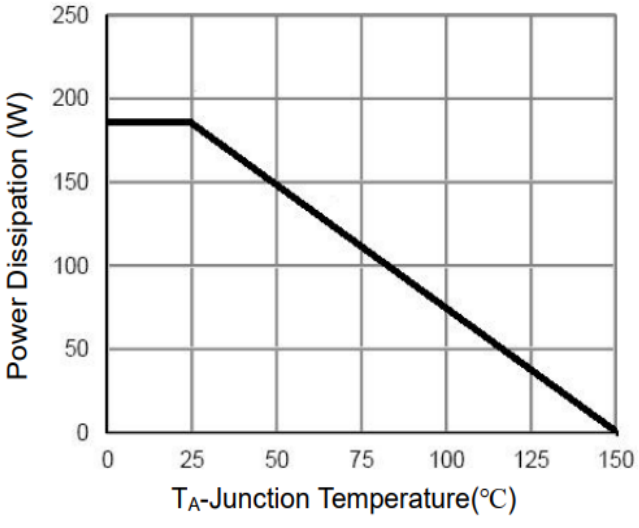
V_{GS}=f(Q_{gate});I_D=25.8A pulsed; parameter: V_{DD}

Diagram 10: Typ. Maximum Safe Operating Area



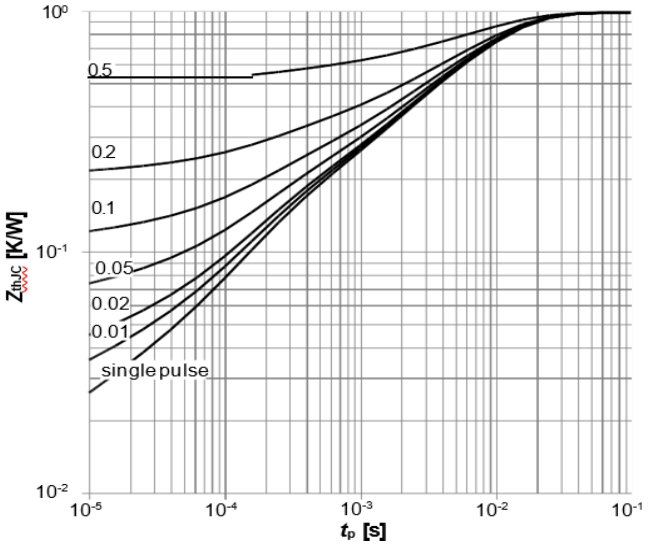
I_D=f(V_{DS}); T_C=25 °C; V_{GS}> 7V; D=0; parameter tp

Diagram 11: Typ. Power Dissipation



P_{tot}=f(T_C);

Diagram 12: Normalized Transient Impedance



Z_{thJC} =f(t_P); parameter: D=t_p/T

5 Test Circuits

Table 8 Diode characteristics

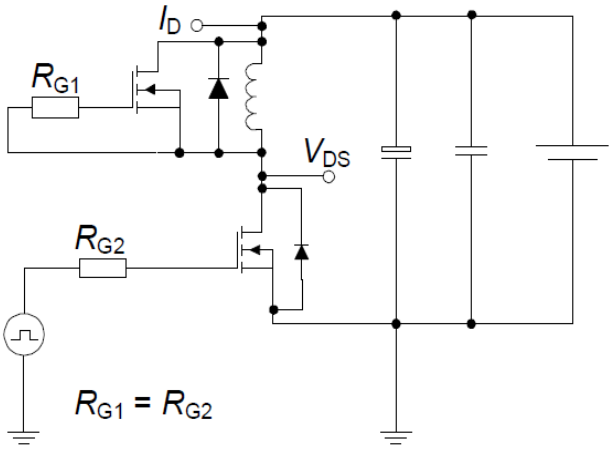
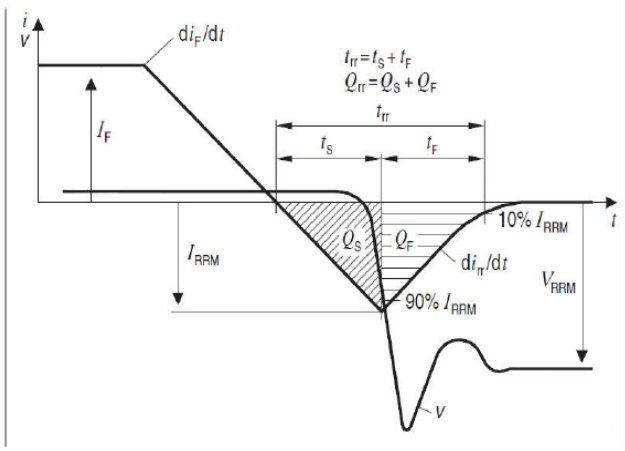
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

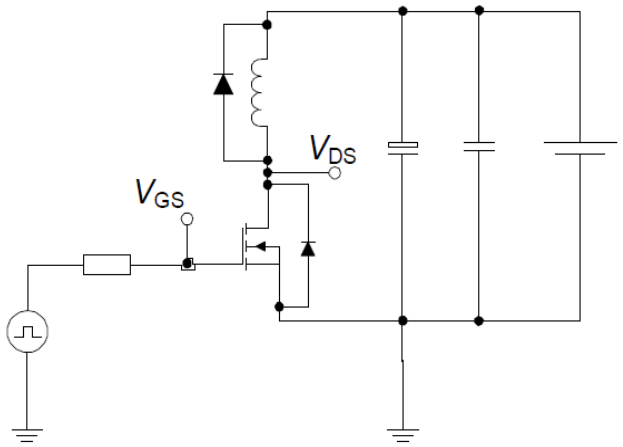
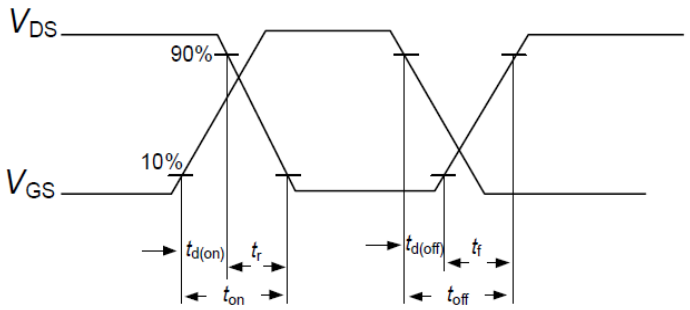
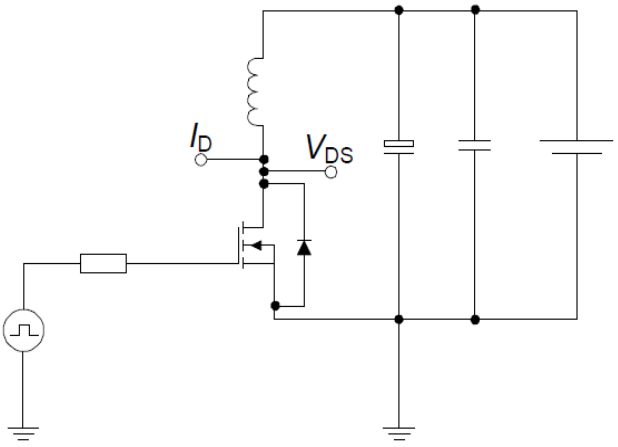
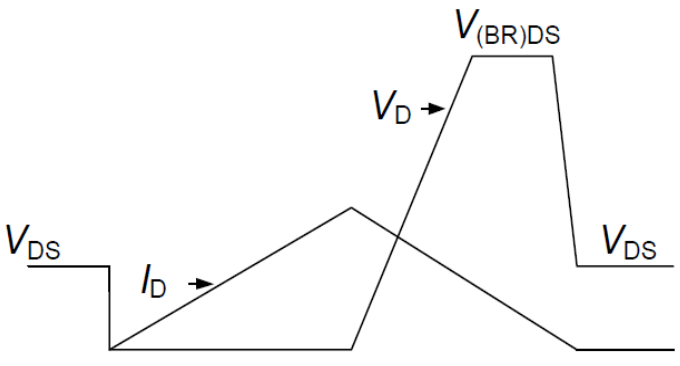
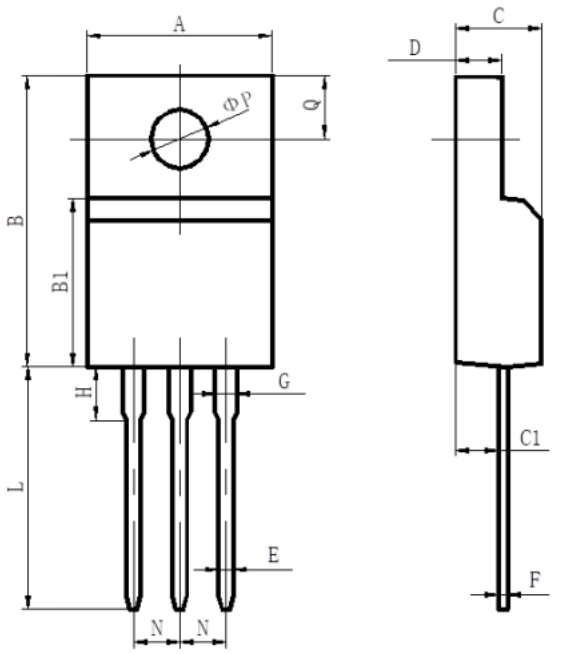
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



项目	规范(mm)	
	MIN	MAX
A	9.70	10.30
B	15.50	16.10
B1	8.99	9.39
C	4.40	4.80
C1	2.15	2.55
D	2.50	2.90
E	0.70	0.90
F	0.40	0.60
G	1.12	1.42
H	3.40	3.80
L	12.6	13.6
N	2.34	2.74
Q	3.15	3.55
ΦP	3.00	3.30

Figure1：Outline PG-TO220F(HT)

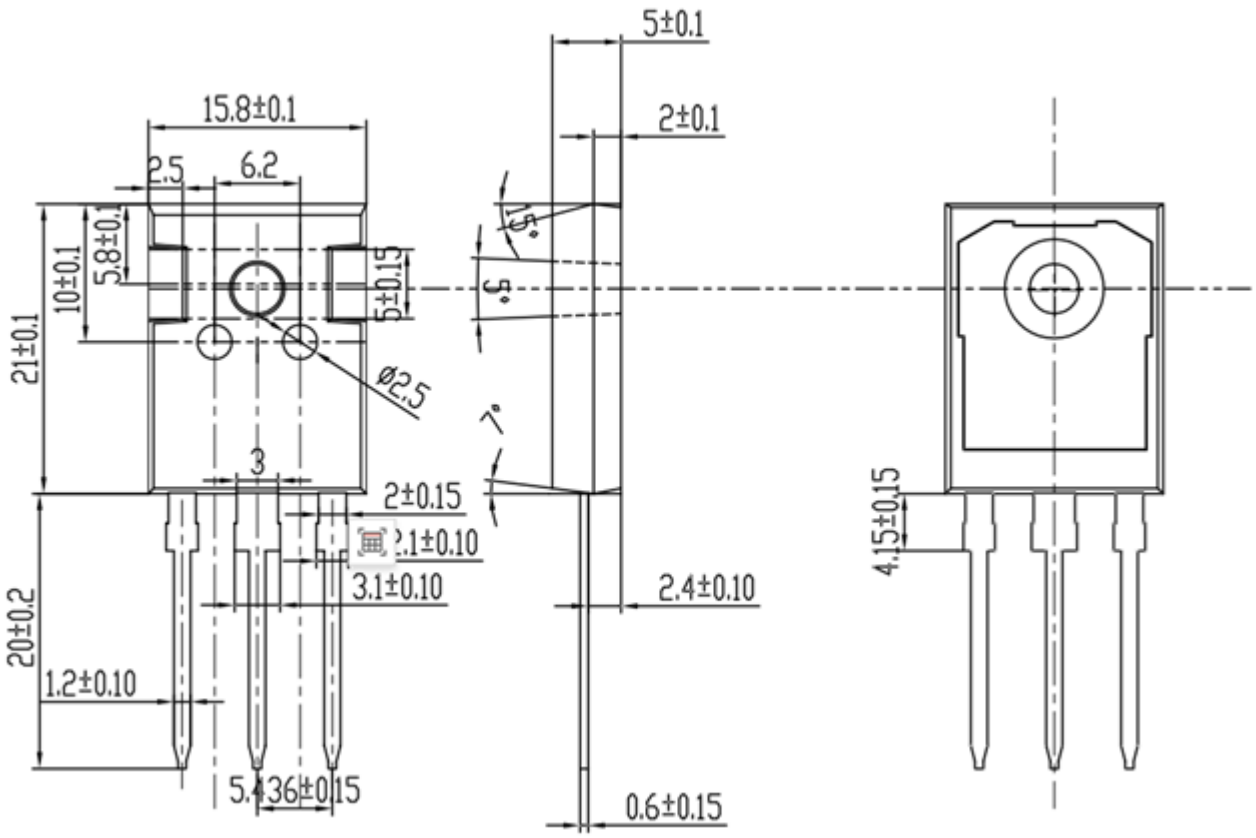


Figure2：Outline PG-TO247(HT)

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2023-07-28	Preliminary version